D^2-*PLC*: Holistic Design and Implementation of High-Datarate Duplex DC Power Line Communication Network

Dongrak Choi, Yubin Choi, Yonghoon Jeong, Jeongyeup Paek, Saewoong Bahk

***Abstract*—Recent advances in electric vehicles, robots, and renewable energy have renewed interest in direct current (DC) *power line communication* (PLC) technology. However, existing DC-PLC systems face from several limitations, including low data rates, lack of support for duplex communication, and the absence of an effective medium access control (MAC) mechanism. To overcome these challenges, we propose D^2-*PLC*, a novel DC-PLC system that features a redesigned physical layer, enabling high-speed duplex communication over a single pair of wires supporting simultaneous power and data transmission. D^2-*PLC* introduces *voltage polarity modulation* (*VPM*) and *current amplitude modulation* (*CAM*) for downlink and uplink communication, respectively. In addition, we develop a custom data link layer and MAC protocols to coordinate communication in a bus topology where multiple slave nodes interact with a single master node (the power source), minimizing the risk of collisions. We implement a fully functional prototype and evaluate on a 5-node testbed as well as via 256-node simulations. Results demonstrate that D^2-*PLC* achieves a maximum data rate of ∼100 kbps–260% improvement over existing solutions–while maintaining 99+% reliability. These findings highlight D^2-*PLC*'s potential to reduce the cost and weight of battery-powered systems such as electric vehicles.**

***Index Terms*—Direct Current Power Line Communication (DC-PLC), Medium Access Control (MAC), Sensor Network**

I. Introduction

POWER Line Communication (PLC) has emerged as a promising solution for systems that require both power delivery and data exchange, such as vehicles, robots, and various electronic devices. Traditionally, maintaining separate lines for power and communication leads to excessive wiring. For example, a single automobile can contain wiring that weighs 60 to 70 kilograms and extends over 4 to 5 kilometers [1]–[3]. Reducing the size and weight of wiring has become a growing priority across industries due to its substantial economic benefits. Leading companies such as Tesla are actively working to minimize wiring harnesses in their vehicle designs [4], [5]. In this context, *Direct Current Power Line Communication* (DC-PLC) is emerging as a promising solution, enabling both power delivery and data transmission over the same set of wires.

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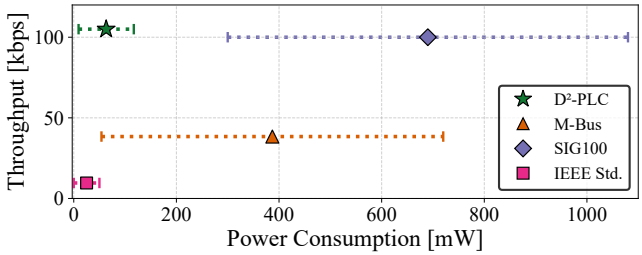


Fig. 1: Maximum throughput and power consumption comparison between D^2-*PLC* and prior DC-PLC technologies.

Over the past few decades, PLC has seen significant advancements, but with more focus on *Alternating Current Power Line Communication* (AC-PLC). Recently, the expansion of DC power infrastructure, driven by the rapid growth of industries such as electric vehicles, renewable energy, and home automation (e.g., HomePlug [6]), has renewed interest in PLC due to its potential to simplify wiring harnesses and reduce system complexity. DC-PLC not only reduces the size, weight, and wiring cost, but also simplifies manufacturing and lowers operational expenses. DC-PLC is applicable to a wide range of systems that operate on DC power and require lightweight, efficient communication, including electric vehicles [7]–[10], robotics [11]–[14], photovoltaic systems [15]–[17], and other DC-powered IoT and 6G devices [18]–[23]. Given these advantages, DC-PLC stands out as a promising technology that will enable the next generation of efficient and cost-effective electronic systems.

Despite the growing interest, the development of DC-PLC technology remains in its early stages. Previous research efforts have faced several key limitations, including low data rates and/or high power consumption (Fig. 1), inability to support duplex communication or simultaneous power and data transfer, and the absence of effective collision resolution mechanisms. Here, duplex communication refers to the ability to transmit and receive data between nodes in both directions, either alternately (half-duplex) or simultaneously (full-duplex), which is essential for acknowledgments, feedback, and coordination. The evolution of communication systems has consistently moved toward efficient duplex communication [24], [25], which is now standard feature in wireless IoT protocols such as Wi-Fi [26], Zigbee [27], and Bluetooth [28]. In this context, enabling high-speed duplex communication over DC power lines is not only a technical challenge but also a necessary step in the natural progression of DC-PLC technologies. As a result, there is a pressing need for a more advanced, robust, and broadly applicable DC-PLC system that can overcome these challenges and unlock the full potential

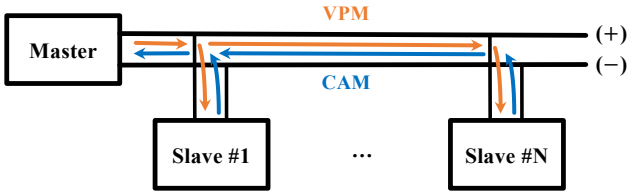


Fig. 2: Master and slaves are connected through a bus topology using a pair of power lines on which data can flow in both directions: VPM (orange) for downlink and CAM (blue) for uplink.

of power line communication in DC-powered systems.

In this work, we propose a novel DC-PLC system called D^2-*PLC*, which achieves high data rates and supports duplex communication. In the D^2-*PLC* architecture, multiple slave nodes are connected to a single master node using a bus topology (Fig. 2). The master node not only delivers power to the slave nodes through a single pair of wires but also simultaneously transmits data over the same power lines. The slave nodes can also transmit data to the master node over the same pair of wires.

However, the design of D^2-*PLC* presents several key challenges. First, the system must ensure stable and reliable power delivery with minimal voltage and current fluctuations during simultaneous data transmission. Second, most existing studies focus on unidirectional downlink communication or low-data-rate duplex implementations. Enabling high-data-rate duplex communication thus requires an entirely new design approach. Third, medium access control (MAC) becomes critical when managing multiple slave nodes transmitting uplink data to the master. This challenge is exacerbated by the fact that slave nodes lack uplink-carrier sensing capabilities as the master continuously supplies power, increasing the risk of collisions. To address these issues, a custom MAC protocol must be designed that operates effectively under these constraints. These challenges must be carefully considered when designing a DC-PLC system's physical and data link layers to ensure reliable, efficient, and scalable communication.

In the physical layer of D^2-*PLC*, we propose two mechanisms–*voltage polarity modulation* (*VPM*) and *current amplitude modulation* (*CAM*)–to enable bidirectional communication between the master and slaves. *VPM* is used for downlink transmission from the master to the slaves, where bits are transmitted by switching the polarity of the voltage on the wire using an H-bridge circuit. Conversely, *CAM* is employed for uplink transmission from the slaves to the master, where bits are transmitted by controlling the amplitude of the current using a symmetric NMOS inverter circuit. These two mechanisms address the first challenge by ensuring reliable communication even in the presence of voltage drops and tackle the second challenge by introducing a novel approach to enable duplex communication.

Moreover, the physical layer alone is insufficient for a fully functional communication system. In the data link layer, we design a standardized frame structure, and adapt techniques from widely used MAC protocols to meet the specific needs of our system, incorporating a collision resolution mechanism to address the third challenge. By leveraging these mechanisms, we establish a new design for a DC-PLC system that supports reliable and high data rate duplex communication.

Real experiments on a 5-node testbed with fully functional prototype implementation demonstrate that D^2-*PLC* supports high-speed, reliable duplex communication. Additionally, simulations are conducted to evaluate the scalability of the system, further validating D^2-*PLC*'s performance and potential under various conditions and scenarios.

The contributions of this paper are as follows:

- We propose D^2-*PLC*, a novel DC-PLC system. We design *VPM* and *CAM* in the physical layer that achieves uplink and downlink speeds exceeding 100 kbps while addressing frame collisions through a MAC protocol in the link layer.
- To validate the feasibility and performance of D^2-*PLC*, we implement fully functional prototypes of both the master and the slaves on actual PCB boards.
- We conduct a comprehensive set of real testbed experiments. Evaluation results demonstrate that D^2-*PLC* enables reliable high-speed duplex communication. We also conduct simulations to confirm the scalability of D^2-*PLC*.

The remainder of this manuscript is organized as follows: §II reviews the related work and the motivation behind our study. §III provides the design of D^2-*PLC*, including its physical and data link layers. §IV describes the prototype implementation, and §V evaluates its performance. Finally, §VI discusses the limitations and future work, followed by a summary in §VII.

II. Background and Related Work

This section presents background information on PLC technology and reviews prior research efforts related to DC-PLC.

A. AC-PLC and DC-PLC

Power line communication can be classified into alternating current (AC) and direct current (DC) PLC based on the power system type, with each developed to suit its respective category [34]–[36]. Both offer unique advantages and challenges, influenced by power transmission characteristics, communication protocols, and application domains. While AC-PLC benefits from the widespread availability of AC power infrastructure, DC-PLC aligns with the growing adoption of DC-powered systems.

AC-PLC is widely used for connecting smart home devices, security systems, and household appliances in residential, office, and commercial environments [37]–[39]. However, AC-PLC faces several challenges due to the inherent characteristics of AC power where voltage and current periodically change in magnitude and direction. Voltage fluctuations at 50 Hz or 60 Hz introduce significant noise and interference, reducing communication reliability and quality [40]. To mitigate these issues, AC-PLC requires complex signal modulation, filtering, noise reduction, and advanced error correction techniques, increasing both system complexity and cost [41]–[45].

In contrast, DC-PLC offers distinct advantages due to its more stable voltage, simplifying signal processing, and improving reliability. Intuitively, DC-PLC is suitable for applications that rely on DC power sources, such as electric vehicles,

TABLE I: Comparison between *D^2-PLC* and prior DC PLC technologies

Technology	PHY throughput (kbps)	Duplex	Voltage Range	Power consumption	Number of nodes	MAC mechanism
IEEE 2847-2021 [29]	9.6	Simplex (downlink)	0–50 V	Low	255	None
M-Bus [30]	0.3 – 38.4	Half duplex	24, 36 V	High	250	Polling
Yamar SIG100 [31]	∼100	Half duplex	10–36 V	High	251	None
PDTM-PLC [32]	0.85	Simplex	10–100+V	High	2∼1000	TDMA
PDRM-PLC [33]	0.002∼0.017	Half duplex	10–100+V	High	2∼1000	TDMA
D^2-PLC	100	Half duplex	12 V	Low	256	Polling/Contention/Reservation-based

renewable energy sources (e.g., solar power systems), or any battery-powered mobile devices like robots and unmanned aerial vehicles (UAVs). DC-PLC effectively reduces wiring complexity in these systems, making it a practical choice for reducing costs.

B. Prior work on DC-PLC

There are two standards that define mechanisms for DC-PLC applications. The IEEE 2847-2021 [29] specifies the physical and data link layers for power and data transfer in low-voltage, high-power environments like renewable energy systems and electric vehicles. It prioritizes cost-effectiveness, reliability, and electromagnetic compatibility (EMC) compliance. This standard defines a topology where a transmitter delivers power and data to multiple receivers in a bus or tree structure, using voltage variations via an H-bridge for encoding. However, it has significant limitations: a maximum data rate of only 9600 bps and support for downlink communication, with no specifications for uplink transmission or MAC protocols to manage collisions. These gaps highlight the need for further development to enable bidirectional communication in DC-PLC systems.

EN 13757-2 [30] is a European standard that defines the physical and link layers of the M-Bus protocol for remote data acquisition from utility meters such as gas, water, and electricity. M-Bus follows a master-slave architecture, enabling bidirectional data transmission through voltage and current variations. However, M-Bus has several limitations. First, the master transmits downlink data by modulating the bus voltage between 36V (logic 1) and 24V (logic 0), making it challenging to provide stable DC power to slave devices. Second, in uplink transmission, it uses current modulation where logic 1 is represented by 1.5 mA, while logic 0 requires an additional 11–20 mA. This added current increases power consumption, which becomes more problematic as the network scales. High current flow may even create the illusion that the slave node is acting as a power source. Furthermore, M-Bus has a limited data rate of 300–9,600 bps. While extended configurations propose support for 19,200 or 38,400 baud, higher speeds introduce signal attenuation and interference, compromising transmission stability. Additionally, M-Bus relies solely on a polling-based MAC protocol and lacks provisions for varying network utilization and number of slave nodes.

The SIG100 transceiver by YAMAR Electronics [31], [46], [47] is a commercially available DC-PLC product. SIG100 modulates universal asynchronous receiver transmitter (UART) or local interconnect network (LIN) byte signals over a DC power line and supports bitrates of up to 115.2 kbps. It enables half-duplex master-slave communication while allowing multiple networks to coexist on a single power line via frequency-division multiplexing, with each network using a dedicated narrowband carrier. To improve noise and interference resilience, SIG100 transmits and receives UART bytes over the DC bus using phase modulation. From a circuit design perspective, it mitigates carrier signal attenuation by incorporating a coupling inductor in the power transfer path. It injects data onto the DC power line via a coupling capacitor. A similar circuit on the receiving side allows for simultaneous power and data recovery. However, reliance on additional coupling components and circuitry not only increases system complexity and cost, but also renders system performance highly dependent on the load's characteristics [48].

I. Mandouraraki *et al.* [32] embeds digital information directly into the power signal by utilizing a built-in output H-bridge circuitry of each power module. This approach eliminates the need for extra coupling circuits. A control unit integrated with the H-bridge converter transmits power source information using rectangular pulse amplitude modulation (PAM) and binary phase shift keying (BPSK), enabling power system monitoring. The receiver first draws power from the power line, senses the current, filters and digitizes the signal, and then extracts the transmitted data using a phase-locked loop (PLL) and demodulator. Multiple power modules transmit data in a designated timeslot via a time division multiple access (TDMA) scheme, achieving a bit rate of approximately 851 bps, sufficient for monitoring PV systems and battery energy storage. However, a MAC protocol operating at this data rate may impose significant constraints on system performance for systems requiring more frequent data exchange.

Building on their previous PLC design, I. Mandouraraki et al. [33] add a feature that allows a remote terminal computer to send digital data, including parameter settings and operational control commands to each power module via the power line. In this approach, data is FSK-modulated and coupled onto the power line using a current transformer, then transmitted to each power module. The modules detect the transmitted data by measuring the current ripple across a current-sensing resistor connected in series with the H-bridge output terminal. However, this method has a significantly lower bit rate, ranging from approximately 2.38 bps to 16.67 bps.

Sung *et al.* [36] propose a time-division multiplexing approach to differentiate the state of the power line into powering and communication phases. However, this work

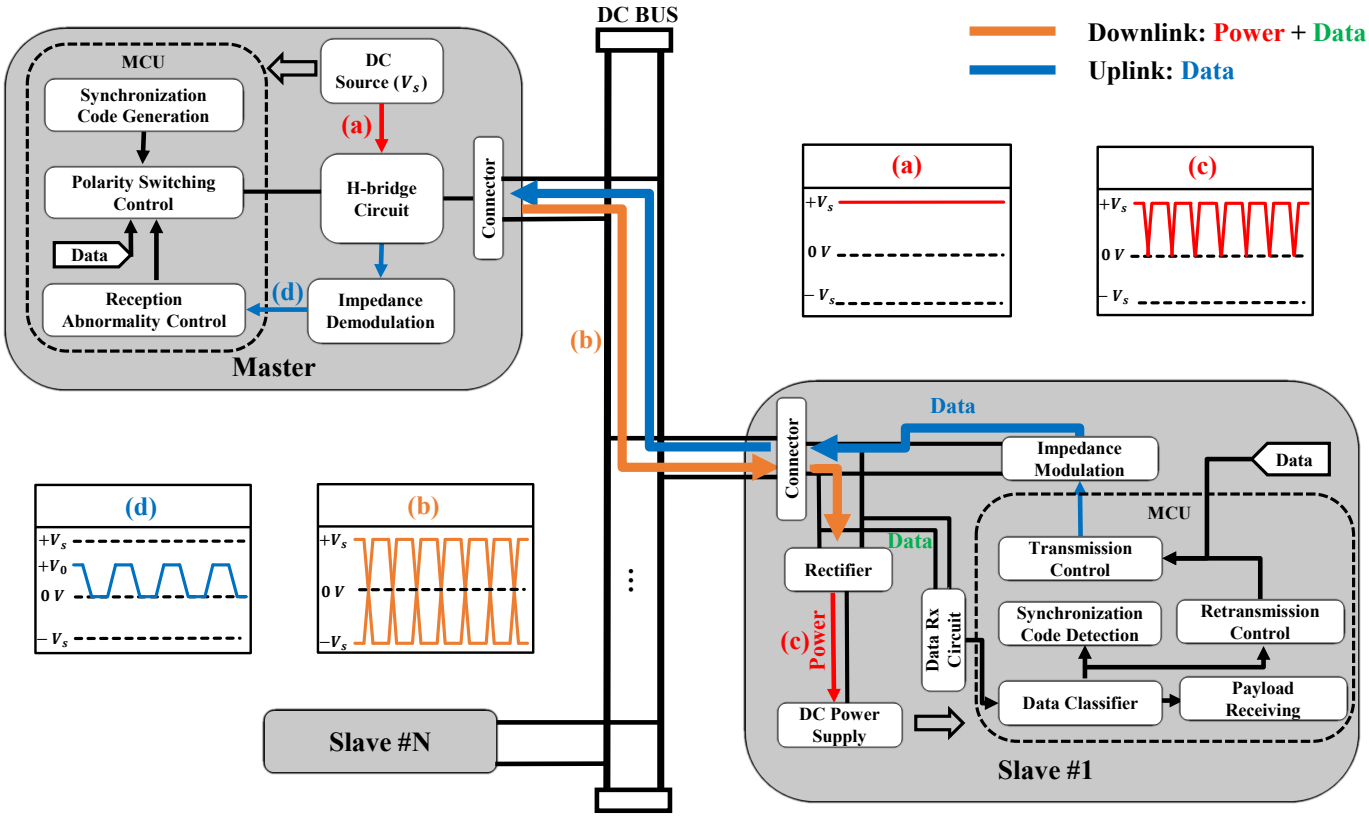


Fig. 3: Overview of D^2-*PLC* communication system. (a)-(d) illustrate the signal waveforms at key stages: (a) DC power signal, (b) downlink power and data combined signal through *VPM*, (c) rectified DC power at the slave, and (d) uplink data signal using *CAM*.

only introduces the concept without evaluating its feasibility. Moreover, since power delivery and communication occur in separate time slots, this DC-PLC system cannot transmit power and data simultaneously. Similarly, Sánchez-Pacheco *et al.* [15] suggest a PV monitoring method that utilizes existing DC power wiring based on DC-PLC and RS232/485 protocols. However, the feasibility of this approach has not been validated through experiments. H. Zhu *et al.* [18] propose that DC-PLC between the supply vessel and autonomous underwater vehicles (AUVs) is achieved by directly superimposing signals onto the power line. However, this approach does not support bidirectional communication and does not propose a MAC protocol.

Finally, some recent studies have proposed using high-frequency carrier modulation to transmit data simultaneously with power over a shared link. One study employs capacitive coupling with inductor-capacitor-capacitor (LCC) compensation [49], and another utilizes a modulation and demodulation scheme over an inductive path [50]. However, these are in the wireless domain, and are not applicable to PLC systems.

III. D^2-*PLC* Design

This section presents the design of D^2-*PLC*. We first provide a high-level description of the system architecture and communication flow, followed by the key functional components including *VPM* and *CAM* in the physical layer and the data link layer mechanisms such as frame structure and MAC.

A. System Overview

Fig. 2 illustrates a high-level view of the D^2-*PLC* system in which a single master node and multiple slave nodes are connected through a bus topology using a pair of power lines. The master node, which functions as the central connection point to the DC power source, transmits both power and downlink data to the slaves. Slave nodes can also transmit data to the master but not directly to other slaves.

Fig. 3 details the functional components within the master and the slaves, together with the signal waveforms at key stages. The master uses *VPM* (§III-B) to modulate data onto the power signal for transmission. At a slave node, the signal is processed by both a rectifier and a data reception circuit. The rectifier converts the signal to DC power, supplying the necessary energy to the system. Concurrently, the data reception circuit demodulates the voltage signal to extract the data. If no errors are detected, the slave passes the received data to the upper (e.g., application) layer.

For uplink communication, slaves transmit data using a variation of impedance modulation, drawing conceptual inspiration from prior load modulation techniques [51]. This method, referred to as *CAM* (§III-C), is adapted for active signaling over DC power lines. The master detects the variation in current, demodulates the signal, and extracts the transmitted data. If there is no error, the master passes the received data to the upper (e.g. application) layer.

However, unlike Ethernet or Wi-Fi, which has a clear channel assessment (CCA) capability, slaves in D^2-*PLC* are

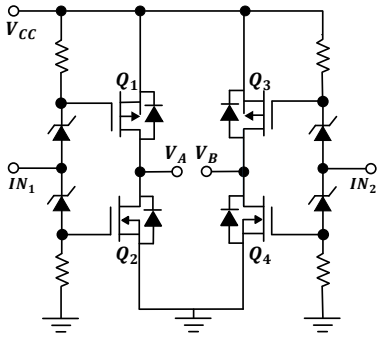


Fig. 4: H-bridge with two PMOS and two NMOS for *VPM*.

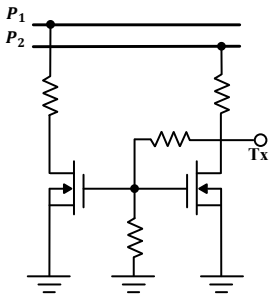


Fig. 5: Impedance modulation module for *CAM*.

unable to detect whether other slaves are transmitting, which can lead to data collisions on the shared power line. To ensure reliable uplink communication, a MAC protocol (§III-E) is required to manage and prevent such conflicts.

B. Voltage Polarity Modulation (VPM)

To enable downlink data transmission, we design *VPM*. *VPM* transmits data from the master to slaves using *differential signaling*, which conveys information through the voltage difference between two wires. When the voltages of the two wires in a DC power line are referred to as V_A and V_B, the potential difference is considered positive if $V_A > V_B$, and negative if $V_A < V_B$. This is how a differential signal represents positive $(+)$ and negative $(-)$ polarities, and the concept holds regardless of whether the voltage difference is expressed as $+V$ or $-V$. By switching the voltage polarity, the master encodes data into the signal pattern and transmits it as a differential signal (see Fig. 3(b)). While the bit representation of *VPM* follows the non-return-to-zero level (NRZ-L) convention, the underlying implementation differs in that polarity is generated through H-bridge–driven differential signaling over a DC power line.

Upon detecting the polarity-switching signal, the slaves decode the transmitted information by interpreting the differential voltage pattern. We use *on-off keying* (OOK) to encode bits where a positive polarity represents bit 1 and a negative polarity represents bit 0. This signal is robust to noise and electromagnetic interference during communication, as its large differential swing $(\pm V)$ provides a high signal-to-noise ratio, making it less susceptible to typical power-line disturbances.

For differential signal generation, the *H-bridge* is a key circuit that reverses the polarity of DC power. Four switching elements, generally transistors, are arranged in a conventional full-bridge configuration that reverses the polarity of the voltage applied to the load. The H-bridge design follows a standard topology commonly used, and in our system, it is repurposed to enable high-speed downlink communication by rapidly toggling the output polarity. This approach takes advantage of the circuit capability to support large voltage swings and fast switching, making it suitable for baseband signaling over DC power lines.

TABLE II: Switch and differential signal results depending on input values in Fig. 4 for *VPM*

Input		Switch				Output		
IN_1	IN_2	Q_1	Q_2	Q_3	Q_4	V_A	V_B	V_{AB}
0	1	On	Off	Off	On	V_{CC}	0	$+V_{CC}$
1	0	Off	On	On	Off	0	V_{CC}	$-V_{CC}$

Fig. 4 illustrates the H-bridge circuit in D^2*-PLC* system (Fig. 3). It has a structure where an inverter circuit consisting of a PMOS connected to V_{CC} and an NMOS connected to the ground in sequence, is mirrored on both sides. To prevent gate damage from voltage transients, Zener diodes are placed at the gate terminals of the H-bridge MOSFETs, enabling safe and stable operation under switching conditions. Due to the surrounding circuitry of the H-bridge, the input values fed into the two inverter circuits through Input 1 and 2 are always complementary (1 and 0) based on the data bits being transmitted. If the input value of Input 1 is 0, the upper PMOS Q1 will be turned off, and the NMOS Q2 will be turned on. As a result, Output A will be set to V_{CC}. Conversely, if the input value of Input 1 is 1, Q1 will turn on, and Q2 will turn off, causing Output A to be set to 0. Since these inverter circuits are connected in a symmetrical structure, the input value of Input 2 determines the on/off states of Q3 and Q4, producing the identical logical behavior for Output B. However, as mentioned earlier, the input values applied to Input 1 and Input 2 are always complementary based on the bit being transmitted. Consequently, the on/off state of each switching element and the voltage applied to each power line depend on the control input values, as summarized in Table II. Output A and Output B are connected to the respective power line wires, and the potential difference between them creates a differential signal. In this way, *VPM* transmits downlink data to the slaves through the power line.

The slave splits the power line input into two parallel paths: one for power rectification and the other for data reception. We utilize a simple diode-bridge rectifier to convert the alternating polarity of the incoming differential signal into a steady DC voltage, which provides power to the slave nodes. In the other path, the data reception circuit measures the polarity between the two power lines and reconstructs the original bitstream based on the polarity direction.

C. Current Amplitude Modulation (CAM)

CAM is designed to enable uplink communication from the slaves to the master. *CAM* also uses OOK modulation to transmit data bits where the *impedance modulation* part in Fig. 3 sends a small current through the power line when transmitting a bit 1, while no current flows for a bit 0. Fig. 5 shows the impedance modulation circuit, which consists of two NMOS transistors. When the data bit is 1, current flows through an additional resistor and into the power line, facilitated by the NMOS transistors. The symmetrical structure of the NMOS transistors ensures that current is correctly transmitted regardless of the polarity of the connected power lines when the data bit is 1. While *CAM* shares a foundational structure with existing load modulation techniques [51], it is

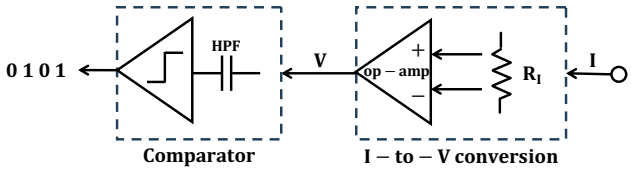


Fig. 6: Illustration of *CAM*'s impedance demodulation.

specifically designed for active uplink communication in a baseband DC-PLC setting. Its use of direct current injection, operation without a carrier, and tight integration with MAC-layer protocols distinguish it from conventional impedance-based sensing or passive feedback systems.

The *impedance demodulation* module in the master node (Fig. 3) can detect the transmitted current. Fig. 6 is its circuit diagram. This module comprises an *I–to–V* conversion unit and a comparator. Based on Ohm's law, the *I–to–V* conversion unit converts the current flowing between the H-bridge and the DC power supply through resistor R_I into a voltage signal. Thus, when a small current is being transmitted to represent a bit 1, it appears as a minimal voltage superposed on the power line voltage. An operational amplifier (op-amp) amplifies the small voltage signal to ensure accurate data extraction. In this manner, the *I–to–V* conversion unit can change the current sent by the slaves into a voltage signal (see Fig. 3(d)), completing the process of preparing the data interpretation. After conversion, the comparator performs simple thresholding: outputs 1 if the input voltage exceeds a reference level and 0 otherwise. Likewise, each slave transmits uplink data by adjusting the current through *CAM*. This approach enables *D^2-PLC* to achieve a datarate of up to 100 kbps, which surpasses the performances of comparable DC-PLC systems.

D. Frame structure

We design a frame structure that suits the modulation schemes (§III-B, §III-C) and performance characteristics (§V) of uplink and downlink communication between the master and slaves in *D^2-PLC*. The default frame length is set to 16 bytes in this work referencing the IEEE DC-PLC standard [29], but it can be a variable-length up to 64 bytes[1]. Within the frame length, we consider different structures for downlink and uplink frames as shown in Fig. 7a and Fig. 7b, respectively. Both frame types share a common 5-byte header shown in Fig. 7c, including a frame number, frame type, slave address, payload size, and cyclic redundancy check (CRC) byte. To reduce frame overhead, we adopt an 1-byte CRC, which offers sufficient error detection capability for a 64 byte frame and is commonly used in other low-power wireless protocols with smaller frame sizes [52]–[55]. In addition, an uplink frame begins with a 5-byte preamble. This is required because *CAM* transmits data by superimposing a small amount of current onto the power line, making it more vulnerable to noise compared to *VPM*. The preamble enhances the reliability of signal detection at the master node, ensuring that uplink transmissions are accurately recognized.

[1]Technically, larger sizes are possible. However, *D^2-PLC* recommends 64 bytes or less due to the reasons we show in §V-B.

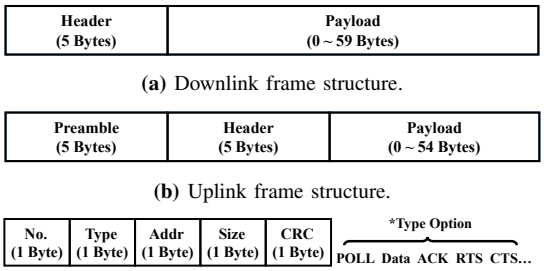


Fig. 7: Structure of downlink and uplink frames. Header format is identical for both.

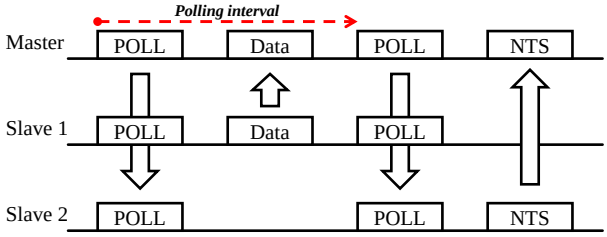


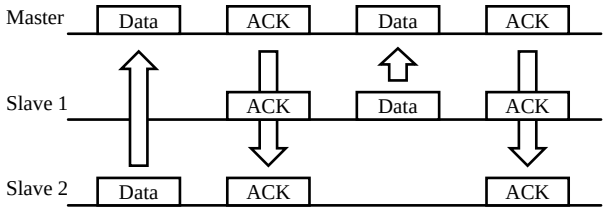
Fig. 8: Polling-based MAC example. Master transmits POLL frames to request uplink data from slaves in order. Slave 1 sends a data frame while Slave 2 sends an NTS (nothing-to-send) frame.

E. Medium Access Control (MAC)

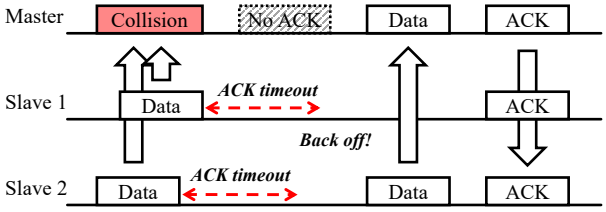
When multiple slave nodes attempt to transmit simultaneously, collisions may occur, preventing the master from correctly receiving the transmitted data. Therefore, it is crucial to coordinate transmissions and implement mechanisms to resolve uplink collisions. To achieve this, we adopt and adapt three well-known MAC scheduling techniques, (1) polling, (2) ALOHA, and (3) reservation-based, for efficient communication. The frame structure follows the format shown in §III-D, which differs by communication direction. All of the frame length is 16 bytes as the default in this paper.

Polling. Fig. 8 illustrates how the master node controls uplink transmissions from slaves through a polling mechanism. In this approach, the master sequentially selects a target slave and physically broadcasts a POLL frame with address information of the target in the header. Upon receiving the POLL frame, each slave checks the address to determine if it is the designated recipient. If so, and if it has data to send, the slave transmits an uplink frame using *CAM*. Otherwise, it sends a nothing-to-send (NTS) frame. After receiving either a data or NTS frame, the master immediately sends the next POLL using *VPM*, continuing the cycle. If no response is received, the master waits for a predefined polling interval before polling the next slave. This master-driven polling mechanism enables orderly and collision-free communication, making it well-suited for application scenarios with centralized control and predictable traffic patterns.

Aloha. Fig. 9 illustrates a modified version of pure ALOHA, adapted to the characteristics of *D^2-PLC*. When a slave has



(a) Slave 1 and 2 successfully complete data exchange without any collision.



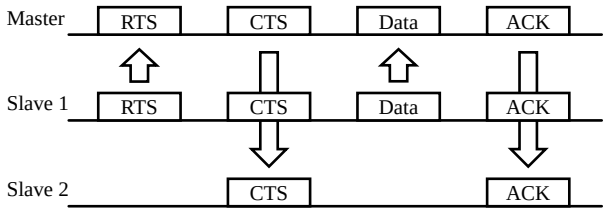
(b) An uplink collision occurs between Slave 1 and 2. Both slaves fail to receive an ACK within the timeout period. Slave 2 retransmits after its backoff timer expires.

Fig. 9: ALOHA-based MAC examples.

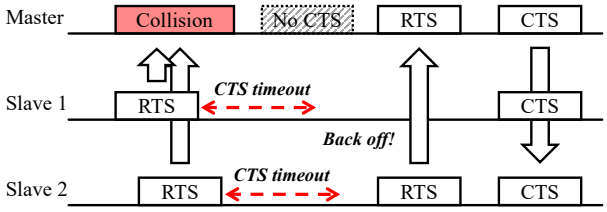
newly generated a frame to transmit, it transmits immediately via *CAM* as illustrated in Fig. 9a. After transmission, it waits for an acknowledgment (ACK) from the master during a predefined timeout period. If the slave receives the ACK, it prepares for the next transmission. However, as shown in Fig. 9b, the slave may fail to receive an ACK due to collisions among simultaneous transmissions or signal loss, resulting in a timeout. To manage retransmissions, the slave sets a backoff timer. Without reinventing wheels, we adopt the popular exponential backoff strategy where the backoff window doubles after each failed attempt, up to a maximum window size of 64. Then for each retransmission, the slave selects a random backoff counter within this window. Using a 10 ms time unit, the total backoff duration is determined by multiplying the counter to this unit. This base unit is set based on empirical observation to allow a full uplink-downlink data exchange with 64-byte frames before retransmission. ALOHA is useful for scenarios with uncoordinated or event-driven transmissions, such as sensor networks with dynamic and bursty traffic, as it supports flexible and asynchronous communication without centralized control.

Reservation-based. Since slaves in *D^2-PLC* cannot hear uplink signals from one another, all slaves act as *hidden nodes* to each other. To address this problem, we implement an RTS/CTS mechanism as shown in Fig. 10. Because a slave cannot detect whether the power line is occupied by another slave, it immediately sends a request-to-send (RTS) frame when it has data to transmit. If the slave receives a clear-to-send (CTS) frame from the master, it proceeds with data transmission and waits for an ACK as illustrated in Fig. 10a. This process allows the slave to reserve the channel prior to sending data.

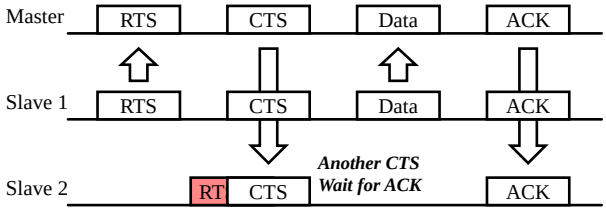
However, if multiple slaves send RTS frames simultaneously, the master cannot decode any of them (Fig. 10b). In such cases, the overlapping uplink signals result in distorted frames, which the master either fails to detect or correctly



(a) Slave 1 successfully completes RTS/CTS exchange with the master, followed by DATA/ACK exchange.



(b) An RTS collision occurs between Slave 1 and 2. Both slaves fail to receive a CTS frame. Slave 1 retransmits the RTS frame upon backoff timer expire.



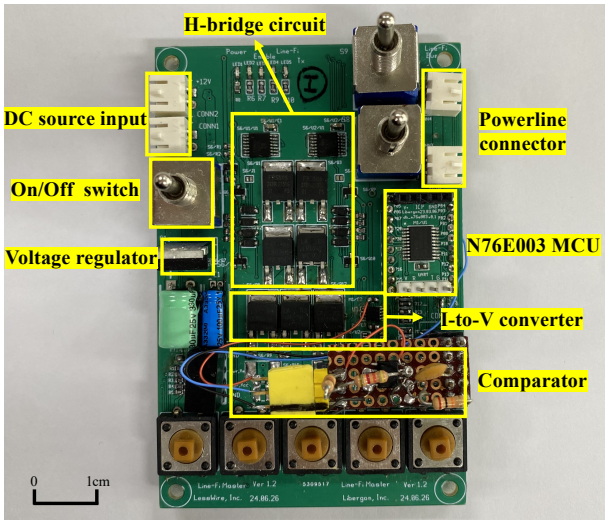
(c) Slave 2 receives a CTS frame intended for another slave immediately after transmitting its own RTS. After receiving ACK for Slave 1, Slave 2 can start the next round for transmission.

Fig. 10: Reservation(RTS/CTS)-based MAC examples.

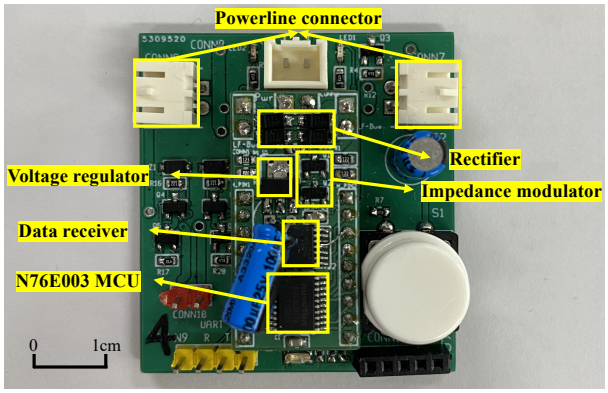
discards based on mismatched header values that violate the expected frame structure. In such cases, the slave does not receive a CTS within the timeout period. In this case, the slave assumes that the channel is under congestion, sets a backoff timer, and retransmits the RTS once the timer expires. On the other hand, a slave may receive a CTS frame intended for another node, as demonstrated in Fig. 10c. Upon detecting this, the slave recognizes the channel as in use, and waits for the ongoing transmission to complete. Once it hears an ACK frame (intended for another node) from the master, it initiates the next round of communication. Because slaves can hear all CTS frames from the master regardless of their intended recipient, they can defer their transmission attempts, effectively reducing the likelihood of collisions. Overall, the reservation-based mechanism is highly effective in shared-medium environments with hidden nodes, such as wireless or power line communication systems. It enhances network efficiency by enabling nodes to reserve the channel in advance, thereby minimizing collisions during transmission.

IV. Implementation

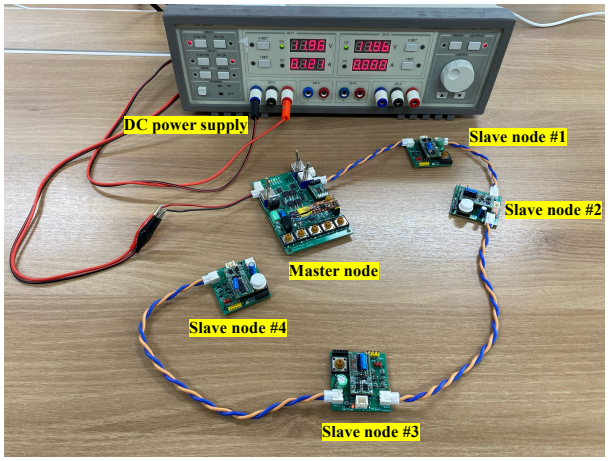
We design and fabricate PCB's for fully-functioning prototypes of the master and slave nodes to validate the feasibility of the proposed *D^2-PLC* system. The prototypes incorporate all the key components and features described in §III.



(a) Master node.



(b) Slave node.



(c) Bus topology example.

Fig. 11: Prototype implementation of D^2-*PLC* system.

Common components. Both the master and slave boards are equipped with the N76E003 microcontroller (MCU) from Nuvoton, which is a cost-effective option priced at approximately \$0.3. This MCU features 18 kB of Flash memory, 1 kB of SRAM, and two UART interfaces. With a package size of 6.5 × 4.4 mm and a power consumption of less than 20 mW during typical operation, it is well-suited for compact and low-power embedded applications. N76E003 is a low-end MCU, and our goal is to implement D^2-*PLC* with minimal hardware resources. The master and slave boards exchange *VPM* and *CAM* signals over power line via the UART interface of the N76E003 MCU [56], which is selected for both timing synchronization and implementation convenience. We utilize 22-AWG copper wire for the power line pairs.

Master. Fig. 11a shows the prototype master board. The board receives power through a 'DC source input' connector. We mount a daughter board on the PCB board to install the MCU, which includes ports for programming and debugging. An 'H-bridge circuit', implemented with two PMOS (IRFR5305 [57]) and two NMOS (IRLR024N [58]), is placed at the center of the board and is used to modulate downlink signals for *VPM*. The switching speed and current tolerance of the selected MOSFETs are well within the required operating range, as confirmed by their datasheet specifications. It inverts the voltage polarity, allowing the HIGH and LOW levels of UART data generated by the MCU to be transmitted through the 'power line connector' located at the top-right corner of the board. 'I–to–V conversion unit' located beneath the H-bridge converts the incoming *CAM* signal into voltage and then digitizes through a 'comparator' circuit with an op-amp (BA4580RFVM-TR [59]). The digitized uplink signal is received by the MCU through the UART interface, enabling successful decoding of the uplink frame.

Slave. Fig. 11b shows the prototype slave node. The two 'power line connectors' on the slave node allow multiple slave nodes to be connected in daisy chain. The incoming power passes through a diode bridge 'rectifier', ensuring a stable DC power supply to the slave MCU. In addition, the 'data receiver' processes the *VPM* signal, converting them into bits (1s and 0s) and forwarding them to the MCU UART port for interpretation. An impedance modulator is used to transmit the *CAM* signal as illustrated in Fig. 5. Fig. 11c shows the experimental setting with PCB boards connected to an actual pair of power lines.

V. Evaluation

We evaluate D^2-*PLC* in terms of throughput, latency, reliability, and the operational behavior of each MAC protocol. We also conduct a scalability analysis through simulations to assess the performance of D^2-*PLC* under varying network conditions.

A. Physical Layer Performance

BER and PHY Throughput. To evaluate the physical layer performance of D^2-*PLC*, we first conduct bit error rate (BER) tests by transmitting 10,000 randomly generated bits in each direction (uplink and downlink) between the master and a slave. Since the MCU implementation operates by exchanging 1-byte UART symbols, every 8 bits are grouped into a single UART symbol for transmission. UART baudrate is set to 230.4 kbps. We repeat the experiment 30 times (300 Kbits per direction in total) and compute the average BER, resulting in 0.019% for downlink and 0.152% for uplink. The small number of bit errors mainly stem from slight imperfections

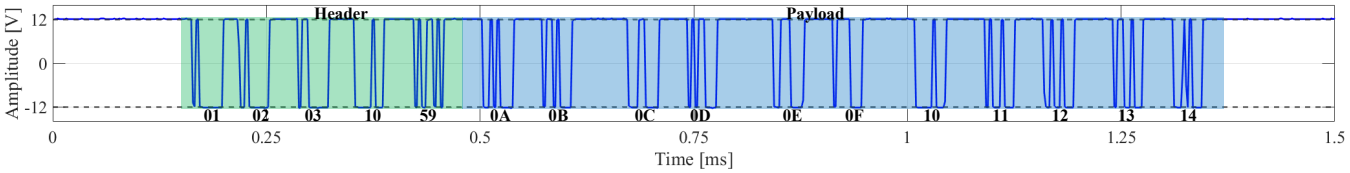


Fig. 12: *VPM* signal on the power line measured at the slave side. Average BER is 0.019% and throughput is 105.3 kbps.

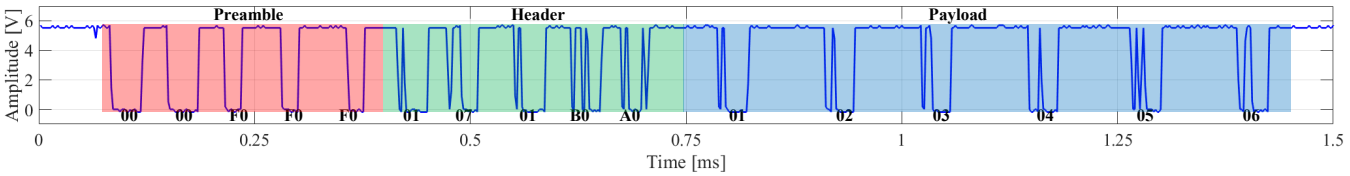
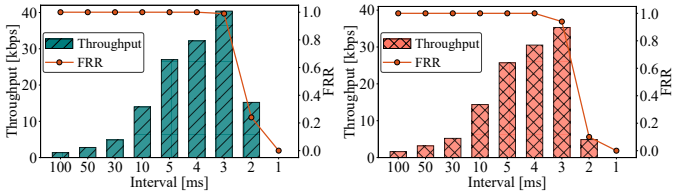
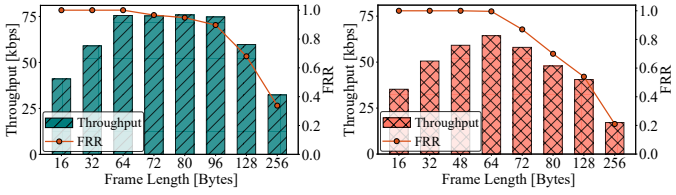


Fig. 13: *CAM* signal measured at the impedance detection module in the master node. Average BER is 0.152% and throughput is 95.1 kbps.



(a) Downlink **(b)** Uplink

Fig. 14: Up-/downlink link-layer throughput and FRR with varying inter-frame transmission intervals.



(a) Downlink **(b)** Uplink

Fig. 15: Up-/downlink link-layer throughput and FRR with varying frame lengths when frames are transmitted back-to-back.

in analog circuits for *VPM* modulation and signal detection at the comparator, which we believe a production-quality hardware can overcome. To accurately measure the physical layer throughput, we capture the transmitted waveforms and their precise time stamps using a PicoScope 2000 Series oscilloscope. Measurements indicate a maximum physical layer throughput of approximately 105.3 kbps for the downlink and 95.1 kbps for the uplink. The slight difference in throughput between up- and downlink arises from differences in decoding complexity and their processing times in the MCUs.

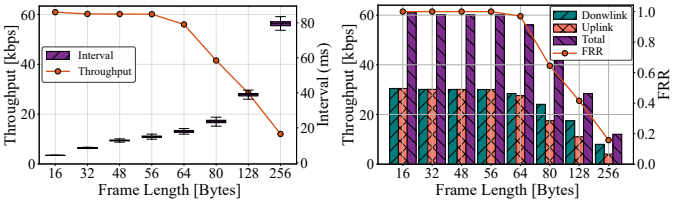
***VPM* and *CAM* Waveforms.** Fig. 12 and Fig. 13 are examples of the downlink (*VPM*) and uplink (*CAM*) signal waveforms, respectively, measured by the oscilloscope when transmitting a 16-byte frame. *VPM* signal is probed directly on the power line, revealing successful transmission of a frame consisting of a 5-byte header and an 11-byte payload. Due to the full $\pm$12 V swing and a voltage deviation of less than $\pm$0.3 V, the *VPM* signal maintains high noise immunity even in the presence of typical disturbances on the DC line. *CAM* signal is obtained after the impedance demodulation unit on the master board, showing the frame structure with a preamble, a header, and a payload. In summary, experimental results validate the physical layer design of D^2*-PLC*, demonstrating that it enables $\sim$100 kbps throughput with high reliability in both directions.

B. Link Layer Performance

Unidirectional Transmission. To evaluate the link layer performance of D^2*-PLC* without contention, we first conduct unidirectional transmission experiments using a master and a slave. We continuously send 16-byte frames at varying inter-frame transmission intervals in each direction while measuring throughput and frame reception rate (FRR). The inter-frame transmission interval, defined as a fixed time gap between the start of two consecutive frames, determines the pacing of transmissions. Fig. 14a and Fig. 14b present the achieved throughput and FRR results for downlink and uplink, respectively. In both cases, the throughput increases as the inter-frame transmission interval decreases (which is obvious), but frame errors start to appear from inter-frame interval of 3 ms and below. This indicates that the time required for frame transmission and reception, including minimal inter-frame spacing for correct signal detection, is approximately 2-3 ms when transmitting a 16-byte frame.

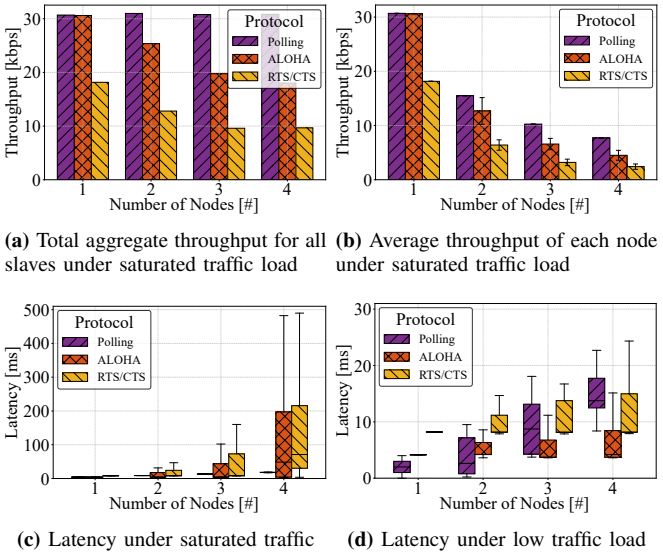
Frame Length. Next, we evaluate the impact of varying frame length on throughput and FRR for unidirectional transmission. In this experiment, we transmit frames back-to-back as fast as possible in each direction. Both downlink (Fig. 15a) and uplink (Fig. 15b) results exhibit similar trends. As the frame length increases from 16 to 64 bytes, the downlink FRR maintains 100% while the uplink FRR drops slightly to 99.8%. Throughput improves accordingly, reaching peaks of 75.5 kbps for downlink and 64.6 kbps for uplink at 64 bytes. Beyond 64 bytes, however, FRR degrades due to non-zero BER, larger frame size, as well as the limited hardware buffer size of the MCU. Thus, throughput also degrades accordingly. The gap between link- and physical layer throughput is due to the inter-frame spacing required to correctly detect and distinguish a frame from non-data power-only transmission.

These observations suggest that a 64-byte frame size provides the best trade-off between transmission efficiency and reception reliability. However, shorter frames, such as 16-bytes



(a) Downlink interval and throughput **(b)** Throughput and FRR

Fig. 16: One-to-one frame exchange experiment.



(a) Total aggregate throughput for all slaves under saturated traffic load **(b)** Average throughput of each node under saturated traffic load

(c) Latency under saturated traffic **(d)** Latency under low traffic load

Fig. 17: Testbed experiment results: Throughput and latency comparison between three MAC protocols.

frame, can be more effective under high contention, as their shorter transmission time reduces the likelihood of collisions. Considering these trade-offs, we adopt a frame length between 16 to 64 bytes which provides a good balance of performance and robustness under various network conditions.

Bi-directional Frame Exchange Experiment. We conduct 1-to-1 frame exchange experiments where the master and a slave continuously alternate transmissions. In this setup, the master and the slave each transmit their frame immediately after receiving a frame from the other side. We then measure the interval between the start times of consecutive downlink frames, which represents the duration of one exchange cycle.

Fig. 16a presents the boxplot of time intervals between two consecutive downlink frames (which includes two frames, down and up), measured using an oscilloscope, as well as the corresponding throughput for different frame sizes. Intuitively, the interval increases with frame length and its variance also increases slightly. For instance, when the frame size is 16, 64, and 256 bytes, the average inter-frame intervals are 4.26 ms, 17.99 ms, and 79.52 ms, respectively, with corresponding min/max of 3.83/4.68 ms, 17.15/20.24 ms, and 75.77/85.48 ms. This trend results from the fact that larger frames not only require proportionally more transmission times but also tend to increase the processing time at both the master and the slave.

In addition, we measure the downlink, uplink, and total effective link-layer throughput, as shown in Fig. 16b. The downlink frames are transmitted with intervals sufficiently long enough to cover the range of intervals measured in Fig. 16a (i.e. max). As shown, the throughput remains relatively stable despite longer frame lengths due to the corresponding increase in transmission and processing time. Beyond 64 bytes, however, the FRR declines due to bit errors accumulating over longer frames as observed in §V-A. Notably, the uplink throughput is slightly lower than the downlink, which aligns with the earlier BER test results. Based on these observations, we set the frame length to 64 bytes or less to balance reliability and throughput, achieving an effective bi-directional link throughput of approximately 60 kbps with the current prototype.

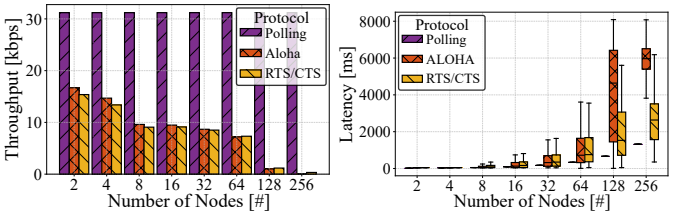
C. Testbed Experiments

Using a testbed with one master and four slaves nodes, we evaluate the uplink throughput and latency of the three MAC protocols with varying slave counts. Results are shown in Fig. 17. Latency is defined as the time elapsed from the frame generation to the reception of the corresponding ACK frame. For the polling scenario where no explicit ACK is used, we substitute the ACK with the arrival of the next broadcast POLL request from the master to estimate up–down round-trip latency. We exclude ACK, POLL, RTS, and CTS frames from the throughput calculation.

Performance under Saturated Traffic. Fig. 17a plots the average total uplink throughput for the three MAC protocols under a saturated traffic scenario where all slaves always have a frame to transmit. Polling MAC maintains a consistent aggregate throughput even as the number of slave nodes increases. In contrast, both ALOHA and RTS/CTS (Reservation-based) show decreasing total throughput as the number of nodes increases. This is because more nodes compete for transmission, which leads to more collisions, retransmissions, and longer backoff delays, reducing the efficiency of the network. Fig. 17b shows the average uplink throughput per slave. With more slave nodes, the average throughput declines across all three protocols, since each node gains less transmission opportunities in a more crowded network.

Fig. 17c plots the latency results. Polling ensures that each slave transmits in a fixed deterministic order at their designated opportunities. Thus the latency increases linearly with the number of nodes. However, the variance remains negligible, and are significantly smaller that other protocols. On the other hand, in ALOHA and RTS/CTS, each collision forces nodes to backoff and retransmit, which amplifies latency. As a result, the latency gap between the polling and other protocols widens with more nodes.

Latency with Low Traffic. In Fig. 17d, we investigate latency under a low traffic load scenario. In this experiment, each slave generates a frame at every 200 ms intervals, with a slight random offset applied to the initial generation time of each node to prevent synchronization. When only one or two slaves are active, polling MAC exhibits the lowest latency. However, as the number of slaves increases, ALOHA and RTS/CTS achieve lower latency since polling MAC requires each slave



(a) Throughput for entire network **(b)** Latency

Fig. 18: Simulation results: Throughput and latency comparison between three MAC protocols under saturated traffic.

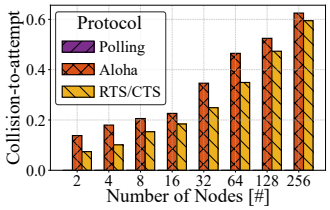


Fig. 20: Avg. number of collisions for each MAC. Note that polling has zero collisions.

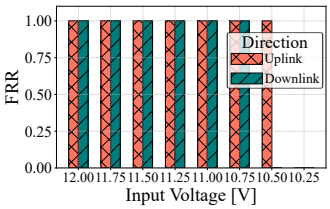
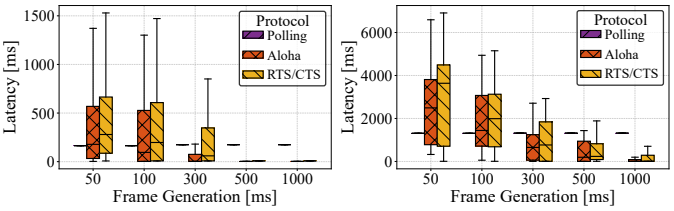


Fig. 21: FRR under input voltage deterioration.



(a) 32 nodes **(b)** 256 nodes

Fig. 19: Latency comparison with varying frame generation intervals for 32 and 256 slave nodes (lower traffic load scenarios).

to wait for its turn, resulting in increased delay proportional to the number of nodes. In contrast, ALOHA and RTS/CTS can send data promptly after frame generation without waiting for their turn, thereby avoiding scheduling delays and delivering data more quickly under lightly loaded traffic.

D. Simulation Results

To analyze the scalability of *D*^{2}*-PLC*, we conduct simulations using a custom-built simulator written in Python that emulates the behavior of *D*^{2}*-PLC* testbed. We set the UART baudrate to 230.4 kbps and the frame length to 16 bytes, consistent with the testbed experiments, while varying the number of slave nodes and the frame generation intervals.

Scalability. Fig. 18 plots the results for the three MAC protocols under a fully saturated traffic load where all slaves always have a frame ready for transmission. Simulation results exhibit similar trends in uplink throughput and latency to those observed in the testbed experiments, and further reveal protocol scalability with increasing number of nodes up to 256 nodes. As shown in Fig. 18a, the aggregate uplink throughput of polling remains stable, while ALOHA and RTS/CTS experience significant degradation as the number of nodes increases. In particular, when the number of slave nodes increases beyond 64, ALOHA and RTS/CTS protocols exhibit severe performance degradation with many nodes rarely succeeding in transmitting uplink data. This is due to intense contention among a large number of slaves, where individual nodes are seldom granted transmission opportunities.

Fig. 18b represents the latency distribution under saturation. ALOHA and RTS/CTS protocols incur higher and more variable latency due to collisions and retransmissions, which intensify as the number of nodes increases. When the number of slaves is 128 or greater, ALOHA exhibits worse latency than RTS/CTS due to aggressive retransmissions and frequent collisions, whereas RTS/CTS reduces unnecessary retransmissions through channel reservation. These results suggest that polling MAC is the most effective protocol for reliable uplink transmission under saturated network conditions.

Varying Traffic Load. We also conduct simulations while varying the frame generation intervals of slave nodes to control the overall traffic load in 32-node and 256-node scenarios. Fig. 19 shows the latency results. With polling MAC, latency remains largely unaffected by the frame generation intervals. In contrast, as the frame generation interval becomes shorter (i.e., under heavier traffic), ALOHA and RTS/CTS show increased latency due to intensified contention for the shared channel. Under light traffic conditions with longer frame intervals, however, contention-based protocols achieve lower latency than polling, as they allow transmission without waiting for a scheduled turn. When comparing the two, ALOHA generally achieves lower latency than RTS/CTS, where RTS/CTS incurs additional overhead due to its channel reservation mechanism.

Fig. 20 plots the collision-to-attempt ratio, calculated as the number of collisions divided by total transmission attempts, at a network frame generation interval of 100 ms. Polling MAC avoids collisions, as only one slave can transmit after a POLL frame is received. In contrast, the collision-to-attempt ratio increases with the number of slave nodes in the other two MAC protocols due to a higher probability of simultaneous transmissions. RTS/CTS has fewer collisions than ALOHA, as it allows a node to reserve the channel while forcing others into a backoff state thereby reducing the likelihood of overlapping transmissions.

Summary. We evaluated the scalability of the system through simulations, observing how throughput and latency vary with changes in network traffic load, node count, and the MAC protocol used. The results reveal that each MAC protocol performs best under specific conditions, highlighting that no single method is universally optimal. These findings not only validate the performance of hardware testbed but also provide insights into the system behavior under a wider range of operating scenarios, suggesting directions for optimizing power line communication in practical deployments.

E. Resilience to Reduced Voltage

We investigate how the voltage level of the DC power source, such as a battery, affects our system. For example, lithium-ion batteries, one of the most widely used DC sources, exhibit a gradual voltage drop during discharge [60]. To

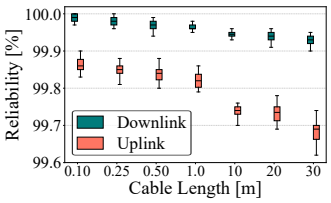


Fig. 22: Reliability comparison by varying cable length.

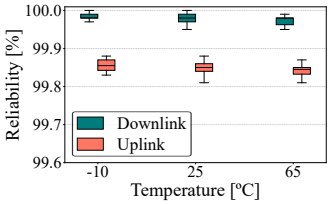


Fig. 23: Reliability comparison by varying temperature.

emulate this behavior, we gradually reduce the input voltage from 12.25 V in 0.25 V steps while continuously sending 16-byte frames unidirectionally and measure the FRR.

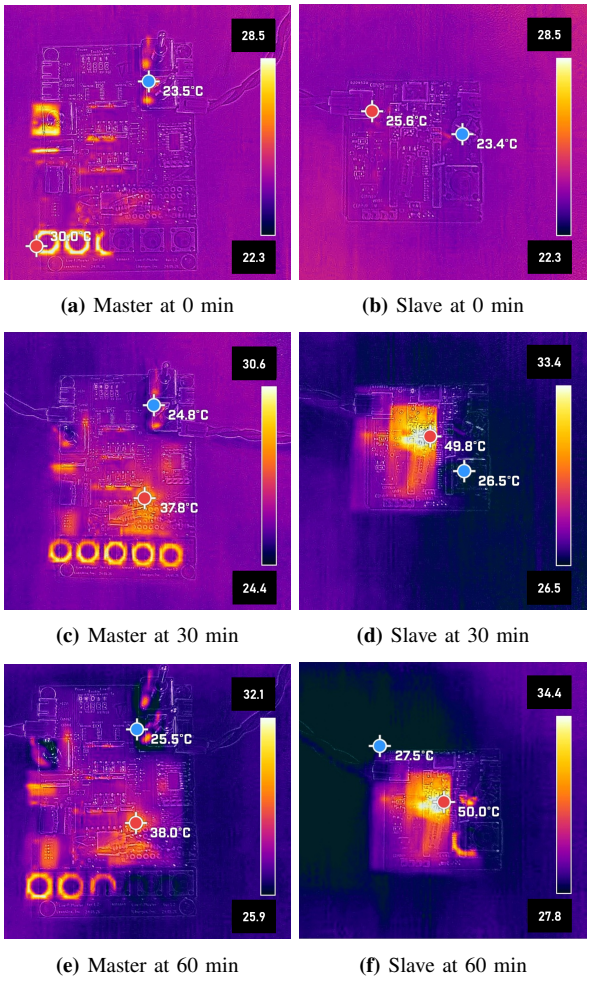
Fig. 21 presents the results. Downlink transmission sustains zero error down to 10.75 V, while uplink achieves error-free down to 10.50 V. This indicates that the system operates reliably even after a 15% drop in voltage from a fully charged battery. Below these voltage levels, however, FRR drops sharply to zero, indicating a clear loss of reliability as the input voltage falls further. These results show that *D*^{2}*-PLC* is robust and reliable under moderately discharged battery, making it well-suited for real-world DC-powered applications such as electric vehicles and robots.

F. Cable Length

To assess the robustness of *D*^{2}*-PLC* over longer power lines, we conduct BER tests while varying the cable length between the master and a slave node from 0.10 m to 30 m. For each length, a node transmits 10,000 bits per trial and repeat the measurement 30 times to obtain the results in Fig. 22. It shows that the downlink consistently maintains over 99.9% reliability across all tested lengths. In the uplink direction, over 99.8% is achieved up till 1.0 m, and slightly below 99.7% at 30 m. The robustness of downlink can be attributed to the differential polarity switching mechanism of *VPM*, which remains largely unaffected by cable impedance. In contrast, *CAM* relies on injecting subtle current variations into the power line. As the cable length increases, so does the total line impedance due to both resistance and inductance. This results in a slightly reduced voltage level at the master-side comparator, potentially leading to rare misclassification of logical states. Nonetheless, the system demonstrates high reliability even under extended cable scenarios, validating its practical viability.

G. Thermal Performance

We examine the thermal performance of the *D*^{2}*-PLC* prototype under various ambient temperature conditions that reflect potential real-world deployment environments. Using a styrofoam insulation box, we create a controlled test chamber and adjust the internal temperature to –10°C, 25°C (room temperature), and 65°C. We conduct 30 BER tests of transmitting 10,000 bits at each condition between the master and a single slave, resulting in a total of 300 Kbits transmitted per direction. The results in Fig. 23 show that the system maintains consistently high reliability across all three conditions. These results suggest that *D*^{2}*-PLC* operates



(a) Master at 0 min **(b)** Slave at 0 min

(c) Master at 30 min **(d)** Slave at 30 min

(e) Master at 60 min **(f)** Slave at 60 min

Fig. 24: Thermal profiles of master and slave boards during 1-hour operation.

reliably under a wide range of thermal environments, making it suitable for use in domains such as automotive systems and smart agriculture.

We also monitor the temperature rise of the boards during active operation at room temperature using a FLIR ONE PRO infrared thermal camera. We operate a polling protocol while connecting a master and a single slave during thermal imaging. As shown in Fig. 24, we capture thermal images at the start, and again at 30 and 60 minutes. On the master board, we observe heat buildup around the resistor near the comparator circuit, reaching approximately 38 °C. On the slave board, the Schottky diode bridge becomes the main heat source, with surface temperatures around 50,°C. However, the temperature tends to saturate between 30 and 60 minutes, indicating thermal stability over time, and these board surface temperatures remain within the operating ranges of our components listed in Table III.

H. Power Consumption

To evaluate the power consumption characteristics of *D*^{2}*-PLC* during simultaneous power and data transmission, we measure the voltage and current on both the master and slave boards under typical operating conditions.

TABLE III: Operating temperature ranges of key components in D^2-*PLC* prototype (from the specifications).

Compoment	Product	Temperature Range [°C]	
		Min	Max
NMOS	IRLR024N [58]	–55	175
PMOS	IRFR5305 [57]	–55	175
Op-amp	BA4580RFVM-TR [59]	–40	105
MCU	N76E003 [56]	–40	105

On the master side, voltage is measured at the DC source output, and current between the supply and board input, capturing total board consumption. When idle, the board draws 12.26 V at 0.6 mA (7.36 mW). During *VPM* downlink transmission, voltage drops slightly to 12.03 V, and current peaks at 5.2 mA (avg. ∼3.5 mA) during polarity switching.

On the slave side, voltage is measured after the rectifier, and current in series with the DC rail. The board maintains 11.70 V throughout. When idle, it draws 0.8 mA (9.36 mW); during *CAM* uplink, current rises up to 10 mA when transmitting logical HIGH, and returns to idle for logical LOW.

The maximum power consumption by communication of D^2-*PLC* is 60 mW at the master and 117 mW at the slave. In comparison, SIG100 [46] reports about 300 mW for both master and slave, while M-Bus [30] shows 264–480 mW at the slave and significantly higher power levels up to watt scale at the master. These results verify that D^2-*PLC* has minimal power overhead, validating its applicability to low-power embedded systems using shared DC lines.

VI. Discussion and Future work

Despite being implemented on an early-stage prototype with a low-end MCU, D^2-*PLC* system already demonstrates a performance that surpasses current state-of-the-art DC-PLC solutions. With a measured datarate of ∼100 kbps in both directions with 99.9% reliability, D^2-*PLC* exceeds the performance of conventional DC-PLC systems and meets the requirements of a wide range of IoT applications including distributed monitoring and low-latency control. Moreover, since the H-bridge and impedance modulation circuits are inherently capable of supporting higher data rates, further improvements in symbol processing or circuit design could yield even greater throughput.

Nonetheless, some limitations remain. Uplink performance degrades slightly as cable length increases (§V-F) due to signal attenuation caused by increased line impedance which reduces the voltage margin at the master-side comparator. Thermal performance (§V-G) remains bounded by the operating limits of the selected components. Under harsher conditions, robustness could be enhanced through refined resistance-capacitance (RC) filtering or digital signal processing (DSP) techniques. Despite these limitations, D^2-*PLC* shows strong potential for real-world deployment in lightweight, low-power applications.

Experimental results indicate that the performance of MAC protocols vary depending on network conditions, such as utilization ratio and number of nodes. Polling-based protocol perform well under high-utilization scenarios by ensuring orderly and collision-free access, whereas contention-based protocols are more effective in low-utilization environments due to their ability to minimize delay. Based on these observations, we plan to develop a hybrid MAC protocol that delivers consistently high performance across a wide range of network conditions. Inspired by prior work such as Z-MAC [61], which successfully combines the strengths of TDMA and CSMA, our approach aims to integrate the structured reliability of polling with the adaptability of contention-based access. The proposed hybrid design will be tailored to reflect the unique characteristics of D^2-*PLC*, enabling adaptive and robust communication even under dynamically changing network conditions.

The current implementation of D^2-*PLC* is limited to the PHY & link layers, and is designed to operate under a bus topology. To support a broader range of communication systems, further architectural development is necessary. As a next step, we aim to develop a transport layer that enables end-to-end communication between nodes, independent of centralized coordination. This would open the door to more flexible network topologies, such as mesh or multi-hop networks, by introducing key functionalities including congestion control and reliable data transfer. Such an extension would significantly expand the applicability of D^2-*PLC*, making it suitable for complex power line infrastructures and IoT deployments. Therefore, an important direction for future work is the design of a lightweight transport protocol that maintains the simplicity and efficiency of D^2-*PLC*, while enabling scalable and decentralized communication beyond the limitations of a traditional bus topology.

VII. Conclusion

We presented D^2-*PLC*, a novel DC power line communication system designed to address the limitations of existing DC-PLC technologies. By leveraging voltage polarity modulation (*VPM*) for downlink and current amplitude modulation (*CAM*) for uplink, D^2-*PLC* enables duplex, high-speed communication over a single pair of wires while simultaneously delivering stable DC power. To support reliable operation in a bus-topology with multiple slave nodes, we also design MAC protocols that can be utilized under various network conditions. We implement a working prototype and evaluate on a 5-node testbed to show that D^2-*PLC* achieves data rates of up to ∼100 kbps with 99+% reliability. These results mark a significant advancement–over 260% improvement compared to prior solutions–and demonstrates its scalability and practicality. We believe D^2-*PLC* has the potential to simplify wiring, reduce weight and cost, and enhance communication efficiency in battery-powered DC-based applications including electric vehicles, robotics, and renewable energy systems.

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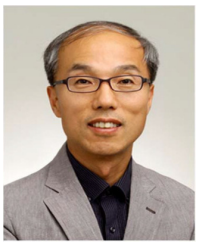

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